WHAT IS CLAIMED IS:

1. A multichip module comprising a plurality of semiconductor chips mounted on said multichip module, wherein each said plurality of semiconductor chips includes at least a plurality of input/output cells connected to a plurality of respective external terminals of the multichip module, and testing means for optionally setting states of said plurality of input/output cells.

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- 2. The multichip module according to claim 1, wherein said test means controls all the states of said plurality of input/output cells that are commonly connected to the same external terminals.
- 3. The multichip module according to claim 1, wherein said test means controls all the states of said plurality of input/output cells of the semiconductor chips.
- 4. The multichip module according to any of claims 1 to 3, 20 wherein said test means includes:
 - a first sets of plural flip-flops of which configuration is based on that of a shift register,;
 - a second sets of plural flip-flops of which inputs are connected to corresponding outputs of the first sets of plural flip-flops; and
 - a selector for selecting a normal signal in a non-test mode, while selecting an output from the second sets of flip-flops in a test mode, so as to give an input/output control signal to said plurality of input/output cells.
 - 5. A multichip module comprising a plurality of semiconductor chips mounted on said multichip module, wherein each said plurality of semiconductor chips includes at least a plurality of input/output cells

connected to a plurality of respective external terminals of the multichip module with being subjected to a boundary scan design, and boundary scan means mounted on said plurality of semiconductor chips for optionally setting states of said plurality of input/output cells.

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6. A multichip module testing method of carrying out a burn-in test for the multichip module which is provided with a plurality of semiconductor chips thereon, each being provided with at least a plurality of input/output cells connected to a respective plurality of external terminals of the multichip module input/output cell, comprising the steps of:

toggling an input/output control signal to one of said plurality of input/output cells connected to one of said plurality of external terminals which is not shared by said plurality of semiconductor chips; and

toggling an input/output control signal with exclusively controlling a state thereof, said respective plurality of external terminals being shared by said plurality of semiconductor chips.